

# Refine Search

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Terms	Documents
L1 same (message or instruction or command)	33

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side by side			result set
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>			
<u>L3</u>	L1 same (message or instruction or command)	33	<u>L3</u>
<u>L2</u>	L1 and (message or instruction or command)	66	<u>L2</u>
<u>L1</u>	processor same initializ\$3 same controller same (disabl\$3 or (single adj1 function))	73	<u>L1</u>

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result set

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L4   L3

0   L4

*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*

L3   L1 same (message or instruction or command)

33   L3

L2   L1 and (message or instruction or command)

66   L2

L1   processor same initializ\$3 same controller same (disabl\$3 or (single adj1 function))

73   L1

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Terms	Documents
(361/683  361/686  370/257  370/453  709/208  710/305  710/104  710/313  710/314  710/315  710/10710/110  711/100  711/147  711/154  712/32  712/36  719/321  719/327  713/1).ccls.	15509

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L5	710/305,104,313-315,10,110;711/100,147,154;361/683,686;713/1;709/208;719/321,327;712/32,36;370/257,453.ccls.	15509	L5
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L4	L3	0	L4
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L3	L1 same (message or instruction or command)	33	L3
L2	L1 and (message or instruction or command)	66	L2
L1	processor same initializ\$3 same controller same (disabl\$3 or (single adj1 function))	73	L1

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Search Results -

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L3 and L5	5

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<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>		
<u>L6</u> L3 and L5	5	<u>L6</u>
<u>L5</u> 710/305,104,313- 315,10,110;711/100,147,154;361/683,686;713/1;709/208;719/321,327;712/32,36;370/257,453.ccls.	15509	<u>L5</u>
<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
<u>L4</u> L3	0	<u>L4</u>
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>		
<u>L3</u> L1 same (message or instruction or command)	33	<u>L3</u>
<u>L2</u> L1 and (message or instruction or command)	66	<u>L2</u>
<u>L1</u> processor same initializ\$3 same controller same (disabl\$3 or (single adj1 function))	73	<u>L1</u>

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IEEE STD	IEEE Standard

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- ☐
- 1. Overview of the Architecture, Circuit Design, and Physical Implementation of a First-Generation Cell Processor**  
Pham, D.C.; Aipperspach, T.; Boerstler, D.; Bolliger, M.; Chaudhry, R.; Cox, D.; Harvey, P.; Harvey, P.M.; Hofstee, H.P.; Johns, C.; Kahle, J.; Kameyama, A.; Keaty, J.; Masubuchi, Y.; Pham, M.; Pille, J.; Posluszny, S.; Riley, M.; Stasiak, D.L.; Suzuoki, M.; Takahashi, O.; Warnock, J.; Weitzel, S.; Wendel, D.; Yazawa, K.;  
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- 2. A universal test and maintenance controller for modules and boards**  
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Bass, J.E.;  
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Digital Object Identifier 10.1109/40.7769  
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**9. Software-only bus encoding techniques for an embedded system**

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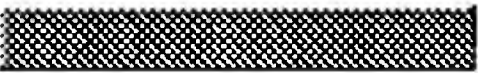
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Jacobson, H.M.; Gopalakrishnan, G.;  
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- 26. Implementation of a MAC-layer protocol (GIG-CSMA/CD) for industrial LAN's and its experimental performance**  
Kapsalis, V.D.; Koubias, S.A.; Papadopoulos, G.D.;  
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Volume 44, Issue 6, Dec. 1997 Page(s):825 - 839  
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- 27. Sensorless vector controller for a synchronous reluctance motor**  
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